Remarks

Claims 1-25 are now pending. Claim 3 is hereby amended for clarification purposes. No new matter is being added.

Claim Rejections--Colwell

Claims 1, 4-8, 15, and 17-18 are rejected under 35 USC 102 as being anticipated by Colwell. Applicants respectfully traverse this rejection.

Claim 1, as previously presented, recites as follows.

1. A **method of compiling a program** to be executed on a target microprocessor with multiple execution units of a same type, the method comprising:
   selecting, by a program compiler, one of the execution units for **testing**;
   scheduling, by the program compiler, execution of **diagnostic** code on the selected execution unit; and
   scheduling, by the program compiler, execution of program code on remaining execution units of the same type,
   wherein said execution of **diagnostic** code on the selected execution unit and said execution of program code on the remaining execution units are scheduled to be performed in parallel.

(Emphasis added.)

As seen above, claim 1 clearly claims a "**method of compiling a program**" where **each claimed step is performed "by a program compiler"**. As is known in the art, a program compiler **transforms source code to object code**.

Moreover, claim 1 recites in the first step that the selection of one of the execution units is "for **testing**" and in the second step that "**diagnostic** code" is scheduled on the selected execution unit. As such, claim 1 relates to the use of a

program compiler to **test** execution units in a microprocessor by scheduling **diagnostic** code to run on a selected execution unit while the remaining execution units continue in parallel to execute program code.

In contrast, Colwell discloses hardware circuitry for processing branch instructions. The citations to Colwell in the rejection of claim 1 are now discussed with specificity one-by-one, as follows.

First, col. 6, lines 46-49 of Colwell is cited against the claim preamble "A **method of compiling a program** to be executed on a target microprocessor with multiple execution units of a same type". (Emphasis added.) Applicants respectfully traverse that this citation teaches or discloses the aforementioned claim language.

Specifically, col. 6, lines 46-49 of Colwell recites as follows. "In accordance with the invention, the hardware architecture described in connection with FIGS. 1-4 is known to the compiler which generates program code for the system." (Emphasis added.) Applicants respectfully submit that the cited reference which states that the hardware architecture is known to the compiler does **not** disclose or teach **a method of compiling a program**.

Second, col. 2, lines 36-44 of Colwell is cited against the claim limitation of "**selecting, by a program compiler**, one of the execution units **for testing**". (Emphasis added.) Applicants respectfully traverse that this citation teaches or discloses the aforementioned claim limitation.

Specifically, col. 2, lines 36-44 of Colwell recites as follows. "The invention features circuitry for processing a plurality of the branch instructions to be executed in parallel and having a hierarchical priority for denoting a tentative order of execution of the instructions, and each processing unit features circuitry for executing a selected plurality of the instructions during a single machine cycle, the selected plurality of instructions including at most one branch instruction, a first and a second branch bank register sets ...." (Emphasis added.) Applicants respectfully submit that the cited reference to circuitry for processing and executing branch

instructions does **not** disclose or teach the claimed step of **a program compiler selecting one of the execution units for testing**.

Third, col. 2, lines 44-58 and col. 6, lines 66-68 of Colwell are cited against the claim limitations of "**scheduling, by a program compiler**, execution of **diagnostic code** on the selected execution unit; and **scheduling, by the program compiler**, execution of **program code** on remaining execution units of the same type." (Emphasis added.) Applicants respectfully traverse that this citation teaches or discloses the aforementioned claim limitations.

Specifically, col. 2, lines 44-58 recites as follows. "... circuitry employing the branch bank register sets for determining whether test conditions associated with a branch instruction are satisfied, circuitry for simultaneously and independently determining a target program counter address for the branch instruction to be executed by the arithmetic processor, circuitry responsive to other processors of the apparatus for determining whether the arithmetic processor is the processor having the highest priority branch instruction with a satisfied branch condition, and circuitry for setting a next instruction address equal to the determined target program counter address of the processor if it has the test condition satisfied highest priority branch instruction." (Emphasis added.) Similarly, col. 6, lines 66-68 recites as follows. "In operation, the compiler uses the Trace Scheduling method to analyze the flow of a program and to predict which paths the program will take." (Emphasis added.)

Applicants respectfully submit that the cited references pertain to processing branch instructions and predicting program flow and do **not** disclose or teach **scheduling diagnostic code on a selected execution unit** (the unit being previously selected for testing) **and scheduling program code on remaining execution units of the same type**, both scheduling steps being performed by a program compiler. Applicants further respectfully submit that the "test conditions associated with a branch instruction" referred to in Colwell relate to conditions that determine which branch is to be taken. In contrast, the claim 1 requires selecting an execution unit **for testing** and scheduling **diagnostic** code to be executed on that unit.

Fourth, col. 1, lines 61-68 of Colwell is cited against the claim limitation of "wherein said execution of **diagnostic code on the selected execution unit** and said execution of **program code on the remaining execution units** are **scheduled to be performed in parallel**." (Emphasis added.) Applicants respectfully traverse that this citation teaches or discloses the aforementioned claim limitation.

In particular, col. 1, lines 61-68 recites as follows. "The method features the steps of processing the sequential instructions for executing a plurality of the instructions during a single machine cycle, the plurality of instructions able to include at least two branch instructions and assigning, during the processing step, a hierarchical priority to any branch instruction to be executed, in parallel, during the single machine cycle." (Emphasis added.)

Applicants respectfully submit that the cited reference pertains to processing at least two branch instructions in parallel and assigning a hierarchical priority to those branch instructions. The cited reference does **not** disclose or teach **scheduling to be executed in parallel the diagnostic code on said selected execution unit and the program code on said remaining execution units.**

For the above-discussed reasons, applicants respectfully submit that claim 1 is patentably distinguished over Colwell.

Claims 4-8 depend from claim 1. Hence, for at least the same reasons as discussed above in relation to claim 1, applicants respectfully submit that dependent claims 4-8 are also patentably distinguished over Colwell. Further reasons for patentability of these dependent claims are discussed below.

Claim 4 is further distinguished over Colwell because the cited reference to col. 11, lines 25-26 of Colwell relates to assigning priority levels for intra-processor unit data transfers. In contrast, claim 4 recites "setting a level of aggressiveness **for scheduling the testing of the execution units**." (Emphasis added.) Applicants respectfully submit that the disclosed priority levels for intra-processor data transfers does **not** teach or disclose the limitation of claim 4.

Claim 5 is further distinguished over Colwell because the cited reference to col. 22, lines 24-32 of Colwell relates to a "'multi-set' cache". In contrast, claim 5 recites "**applying an aggressiveness-dependent algorithm to determine when to schedule all available units for execution of the program code and when to schedule parallel execution of the program code and the diagnostic code**." (Emphasis added.) Applicants respectfully submit that the disclosed multi-set cache does **not** teach or disclose the limitation of claim 5.

Claim 6 is further distinguished over Colwell because the cited reference to col. 11, lines 31-34 of Colwell relates to a two-bit field representing "the state of bus usage by the processor." For example, the field can be "11 = no buses being used." (Emphasis added.) In contrast, claim 6 requires that a lowest level of aggressiveness for scheduling the testing of the selected execution unit comprise **turning off said testing of the selected execution unit**. Applicants respectfully submit that the disclosed field which may indicate "no buses being used" does **not** teach or disclose the limitation of claim 6.

Claim 15 is an independent claim to a computer-readable medium with limitations which are similar to the limitations of method claim 1. Hence, applicants respectfully submit that claim 15 is patentably distinguished over Colwell for at least the same reasons as discussed above in relation to claim 1.

Claims 17 and 18 depend from claim 15. Hence, for at least the same reasons as discussed above in relation to claim 15, applicants respectfully submit that dependent claims 17 and 18 are also patentably distinguished over Colwell.

Claim Rejections--Colwell in view of Raina

Claims 9-14 and 19-24 are rejected under 35 USC 103 as being unpatentable over Colwell in view of Raina. Applicants respectfully traverse this rejection.

Claims 9-14 depend from claim 1. Hence, for at least the same reasons as discussed above in relation to claim 1, claims 9-14 are also patentably distinguished over Colwell in view of Raina.

Claims 19-24 depend from claim 15. As such, for at least the same reasons as discussed above in relation to claim 15, claims 19-24 are also patentably distinguished over Colwell in view of Raina.

Additional reasons as to why these dependent claims are patentably distinguished over Colwell in view of Raina are discussed as follows.

Regarding claims 10 and 20, a portion (col. 3, lines 19-22) of Raina is cited which pertains to the testing of multiple processor cores by comparing output signals if the input signals are the same. In contrast, claims 10 and 20 require that" the scheduled diagnostic code performs diagnostic operations from a **test pattern** comprising operations with **known expected results**." The cited portion of Raina does **not** teach or disclose such a test pattern with known expected results. On the contrary, applicants respectfully submit that Raina performs its comparison operation precisely because the results are unknown.

Regarding claims 12 and 22, a portion (col. 3, lines 15-22) of Raina is cited which pertains to the testing of multiple processor cores by comparing output signals if the input signals are the same and where "... the test result is either a pass or a fail indication." In contrast, claims 12 and 22 require that "the scheduled diagnostic code **jumps to a fault handler** if the compared results are different." (Emphasis added.) Applicants respectfully submit that the cited portion of Raina does **not** teach or disclose such jumping to a fault handler.

Regarding claims 13 and 23, a portion (col. 3, lines 17-19) of Raina is cited that states "If all of the input signals do not have the same logic value, then a disable state value is output, at state 106." (Emphasis added.) Applicants respectfully submit that this state disables the comparison of the output signals. In contrast, claims 13 and 23 require "code to **remove a faulty execution unit from use**...."

(Emphasis added.) Applicants respectfully submit that the disable state of Raina does not remove a faulty execution unit from use.

Regarding claims 14 and 24, the portion (col. 3, lines 17-19) of Raina is again cited that states "If all of the input signals do not have the same logic value, then a disable state value is output, at state 106." (Emphasis added.) Applicants respectfully submit that this state disables the comparison of the output signals. In contrast, claims 14 and 24 require "code to **perform a system halt**...." (Emphasis added.) Applicants respectfully submit that the disable state of Raina does **not** perform a system halt.

Claim Rejections--Colwell in view of Murthi

Claims 2, 3, 16 and 25 are rejected under 35 USC 103 as being unpatentable over Colwell in view of Murthi. Applicants respectfully traverse this rejection.

Claims 2 and 3 depend from claim 1. Hence, for at least the same reasons as discussed above in relation to claim 1, claims 2 and 3 are also patentably distinguished over Colwell in view of Murthi.

Claim 16 depends from claim 15. As such, for at least the same reasons as discussed above in relation to claim 15, claim 16 is also patentably distinguished over Colwell in view of Murthi.

For similar reasons as discussed above in relation to claim 1, claim 25 is patentably distinguished over Colwell in view of Murthi.

Applicants respectfully submit that the cited BSP (bootstrap processor) of Murthi does not teach or disclose the claimed limitation which pertains to selection of a unit for diagnostic testing **by a program compiler**. Hence, applicants respectfully submit that Murthi does **not** disclose or teach the limitations of claims 2, 3, 16 and 25.

Amended Claim 3

Regarding amended claim 3, claim 3 is now amended so as to further clarify that **source code is input** into the program compiler, and **object code is output** by the program compiler.

In addition, claim 3 further clarifies that **the scheduling of code by the compiler is performed prior to execution of code by the target microprocessor**.

Therefore, the claim language of amended claim 3 makes it explicitly clear that the cited art of Colwell, Raina, and Murthi do **not** read on the limitations discussed above in relation to independent claim 1.

Advantages

Applicants further note the following advantages, as described on page 11, lines 5-16, of the present application.

> **An embodiment of the present invention advantageously makes fault tolerant features available on lower-end systems. Previously, such fault tolerant features may have been unavailable on such lower-end systems due to their cost-sensitive nature.**
>
> **A compiler providing fault checking in accordance with an embodiment of the invention is not limited to a particular CPU architecture. A compiler for any appropriate CPU may be so modified, provided that the CPU has multiple functional units of the same type that may be scheduled in accordance with an embodiment of the invention.** Furthermore, while the above discussion describes the invention in the context of compiling user code, the invention may also be applied to the compilation of non-user code, such as, for example, kernel code for an operating system.

(Emphasis added.)

Conclusion

For the above-discussed reasons, applicants respectfully submit that each of the pending claims is patentably distinguished over the cited art. Favorable action is respectfully requested.

The Examiner is also invited to call the below-referenced attorney to discuss this case.

Respectfully Submitted,

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